

AD9671EBV SETUP INSTRUCTIONS

EQUIPMENT NEEDED

Analog signal source and antialiasing filter

2 switching power supplies (6.0 V/12.0 V, 2.5 A) CUI EPS060250UH-PHP-SZ, provided

Linear bench top dc voltage source (0 V to 1.6 V), not required for CW Doppler mode

PC running Windows® 98 (2nd edition), Windows 2000, Windows ME, Windows XP, or Windows 7

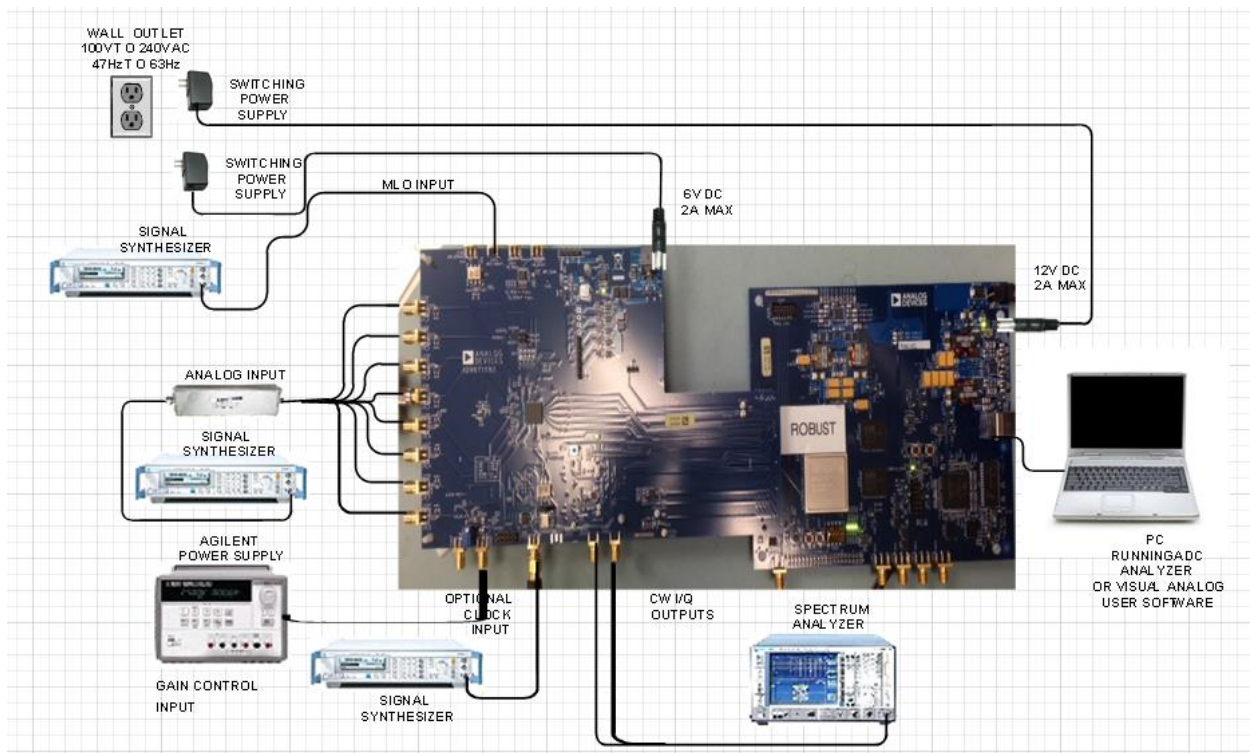
USB 2.0 port, recommended (USB 1.1 compatible)

AD9671 evaluation board (AD9671EBZ)

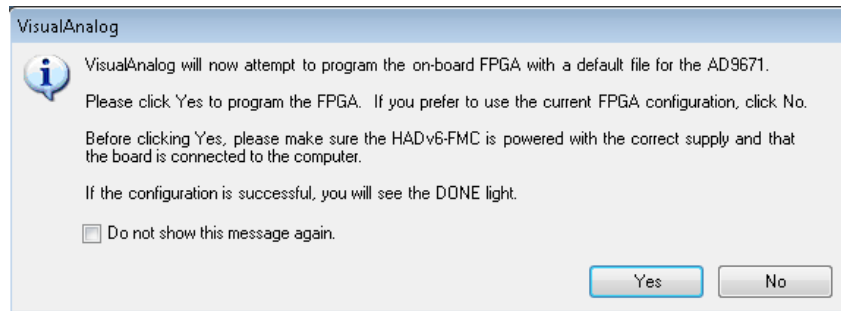
HSC-ADC-EVALEZ FPGA-based data capture kit

For CW Doppler mode: spectrum analyzer

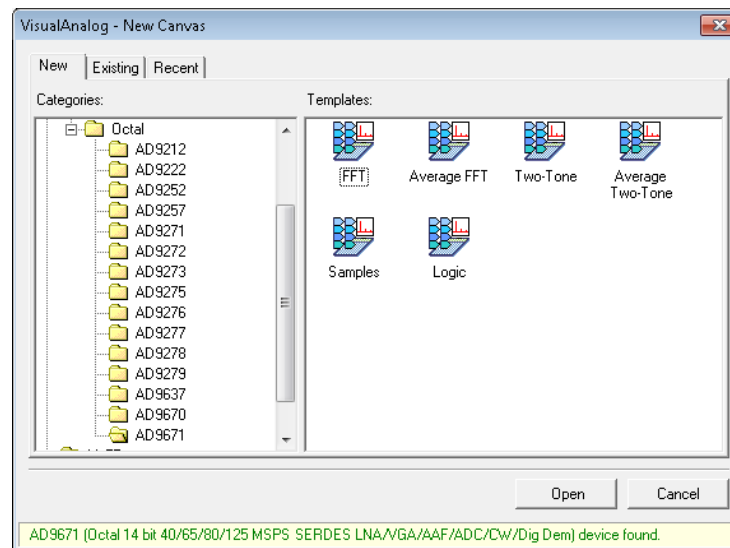
1. Install VisualAnalog (from www.analog.com/fifo).
2. Install SPIController (from www.analog.com/fifo).
3. Plug-in USB cable and 12V adapter to power up the FPGA data capture board and the 6V adapter to power up the AD9671 evaluation board. Example setup:



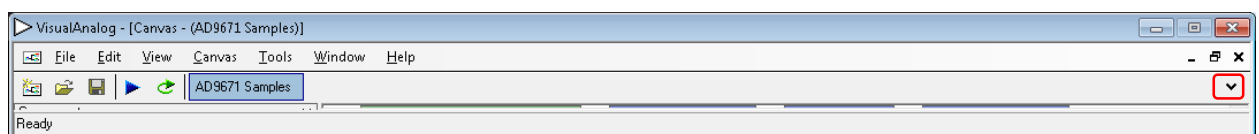
4. Launch VisualAnalog, which will attempt to program the FPGA with the default file associated with the detected AD9671 board. The CONFIG_DONE LED should now be illuminated on the FPGA board.

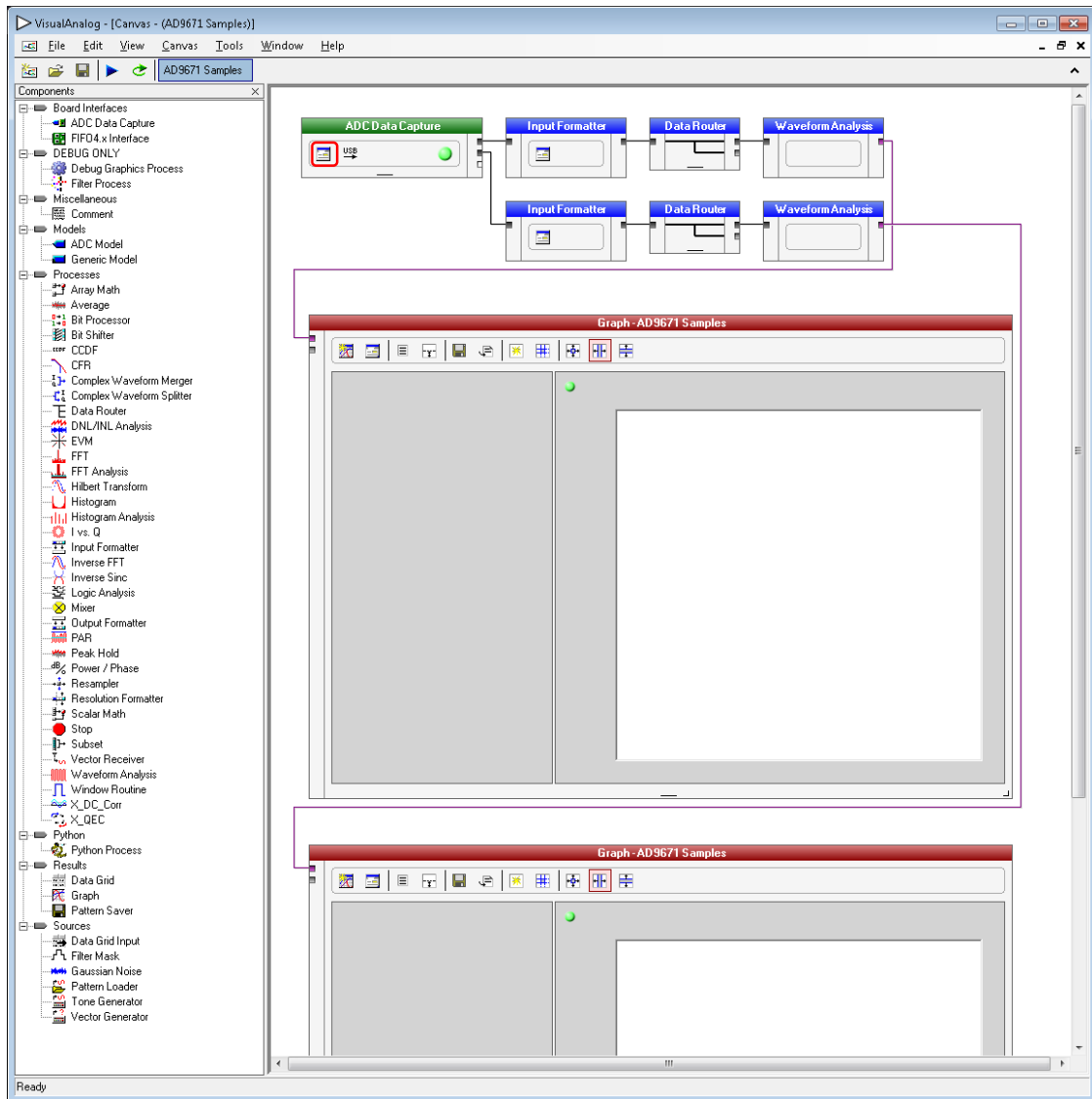


- The templates listed under AD9671 can be used. The Samples canvas shows output versus sample count.

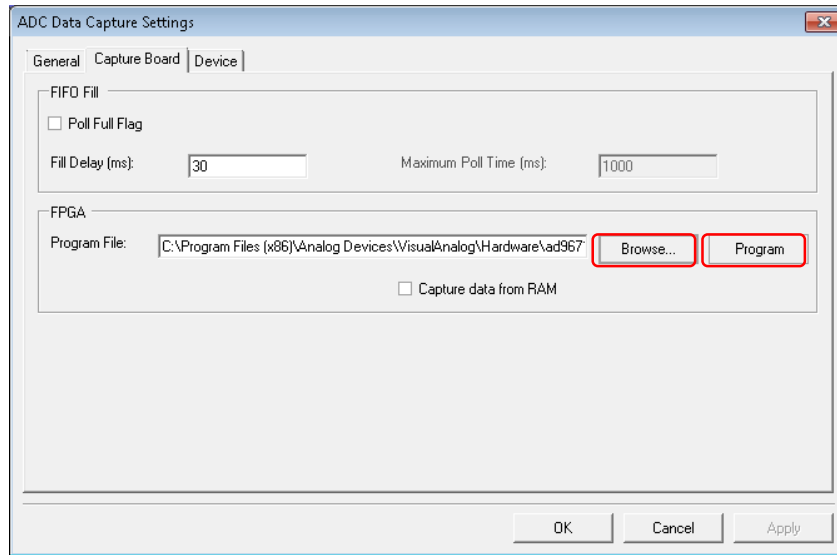


- VisualAnalog opens only showing the task bar. Click on the down arrow on the right side to expand the canvas to see the signal processing flow.

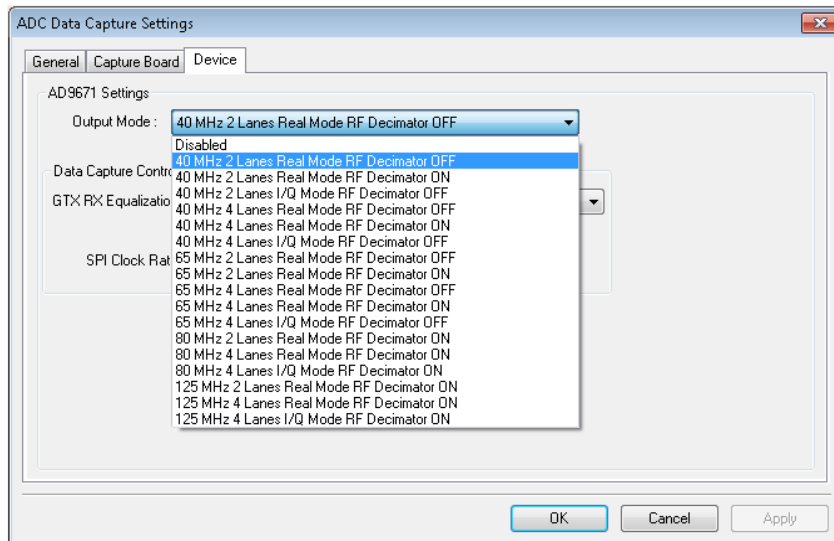




7. If there is a need to reprogram the FPGA after VisualAnalog was launched (e.g. the boards were powered up after VisualAnalog was launched) then open the settings menu on the ADC Data Capture block on any canvas, as marked with the red box in the above figure. Under the Capture Board tab on the ADC Data Capture dialog, Browse to select the bin file `ad9671_evalez06132014_0921am.mcs` and hit Program. The CONFIG_DONE LED should now be illuminated on the CVT-ADC-DC01Z board. Select OK to close that window.

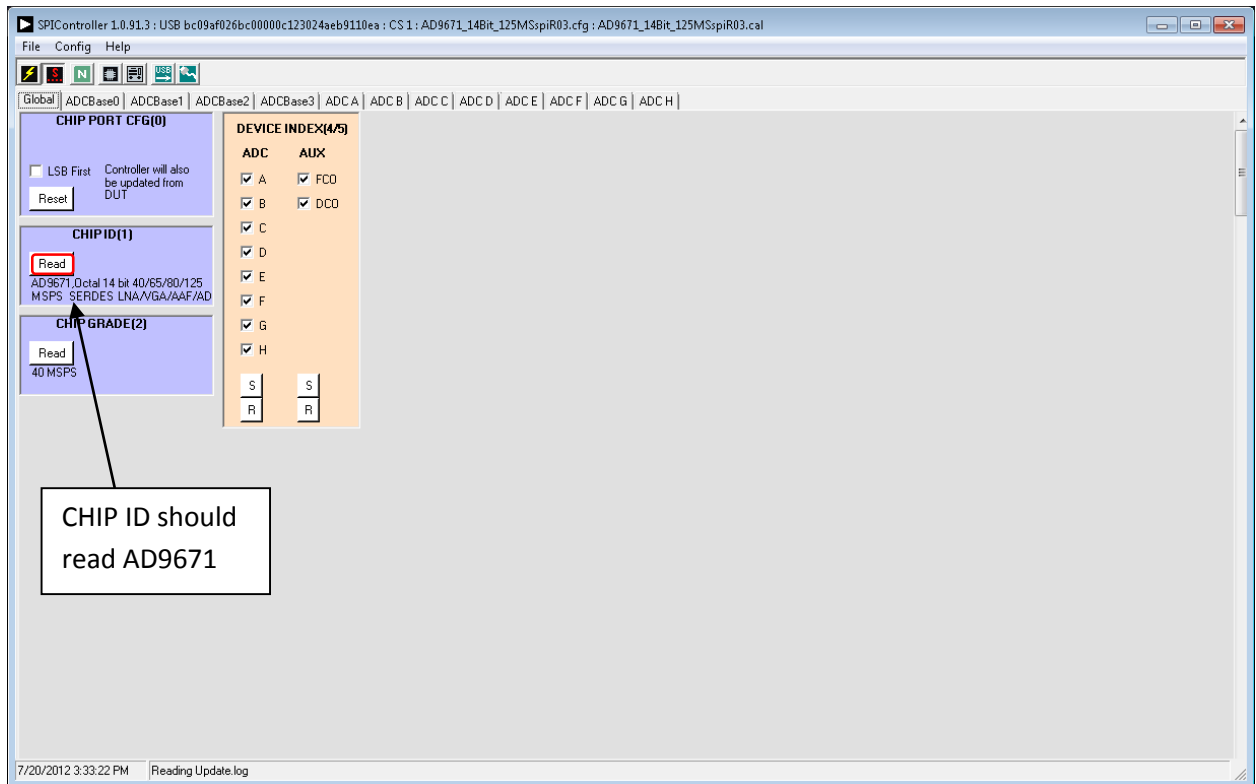


8. Select the output mode from under the “Device” tab of the ADC Data Capture Settings dialog, as shown below. The default clock crystal on the AD9671 board is 40 MHz; if a different speed mode is intended then an external clock can be provided after setting the clock jumper “J301” on the AD9671 board to off state, to allow the external clock source to be connected.



9. Launch SPIController. Select the AD9671 cfg file from the list.
10. In SPIController, under File select Download Files from FTP Site and click OK to backup the files and proceed with the download. This may take a few moments. SPIController will launch when this completes.

11. The Open cfg browser should open and select AD9671_14bit_125MSspiR03.cfg



12. Under Config menu select Launch Memory Map Dialog. This will launch the Coefficient and Profile memory loader as well as a way to select pre-stored demodulation and decimation profiles.

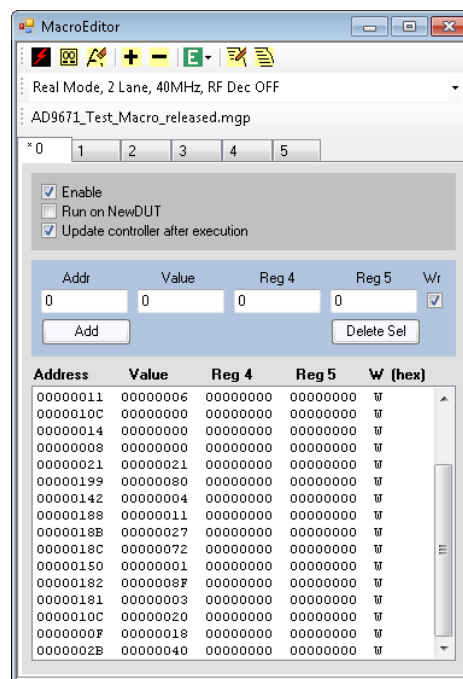
Reads the memory on the device and saves it to a file.

Updating Profile # selects a new decimation rate and coefficient pointer.

Demodulation frequency can be changed by update Demod and Sample Freq.

13. On the main SPIController window, select MacroGroup Open under File. Browse to C:\Documents and Settings\All Users\Application Data\Analog Devices\SPIController\Macros\AD9671_Test_Macro_released.mgp.
14. Under Config menu select Launch Macro Editor. The MacroEditor enables a batch write of SPI registers to setup the part for continuous run mode.

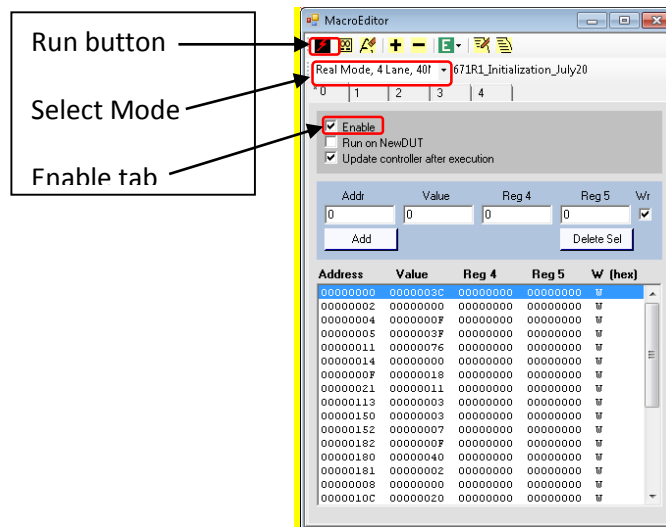
Register	Functions
0x00	SPI Reset
0x02	Set Speed Mode
0x04, x05	Enable/disable channels
0x113	Enable/bypass digital filters, demodulator, decimator
0x011	LNA/VGA gain settings
0x10C	Set index profile
0x014	Offset Binary enable
0x008	TGC run mode
0x021	Set #bits, #lanes
0x199	Enable sample clock counter
0x142	Enable Serial Initial Lane Alignment Sequence
0x188	Enable Start Code
0x18B	Set start code word (MSB)
0x18C	Set start code word (LSB)
0x150	Set JESD204B Scrambler, # lanes
0x182	Set PLL auto configure
0x181	Set PLL N-divider
0x10C	Set SPI TX_TRIG
0x00F	Filter cutoff frequency, band
0x02B	Set analog LPF and HPF to defaults, tune filters



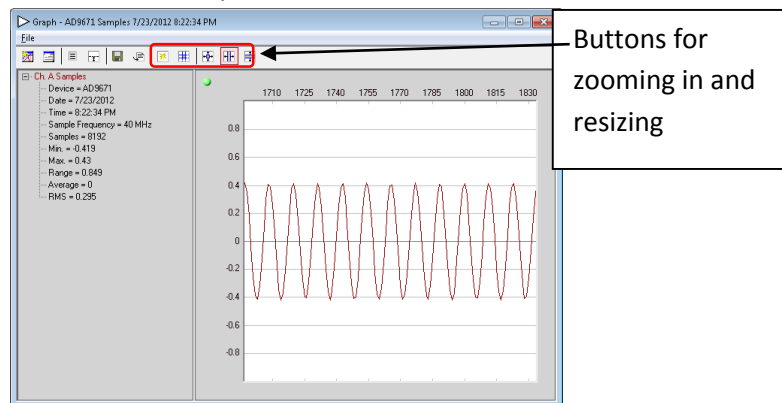
15. To run the macro select one of the tabs, while the internal or external clock should match the speed mode selected. The macro supports the following modes:
 - a. Real Mode, 2 Lane, 40MHz, RF Dec Off – this mode has 4 channels per lane, speed mode set to 40MSPS and all digital post processing disabled including RF decimation filter.

- b. Real Mode, 2 Lane, 40MHz, RF Dec On – this mode has 4 channels per lane, speed mode set to 40MSPS and all digital post processing disabled except RF decimation filter, which is enabled.
- c. Real Mode, 2 Lane, 65MHz, RF Dec Off – this mode has 4 channels per lane, speed mode set to 65MSPS and all digital post processing disabled including RF decimation filter.
- d. Real Mode, 2 Lane, 80MHz – this mode has 4 channels per lane, speed mode set to 80MSPS and the RF decimator enabled.
- e. Real Mode, 4 Lane, 80MHz – this mode has 2 channels per lane, speed mode set to 80MSPS and the RF decimator enabled.
- f. Real Mode, 4 Lane, 125MHz – this mode has 2 channels per lane, speed mode set to 125MSPS and the RF decimator enabled.

The “lightning bolt” button runs the writes.

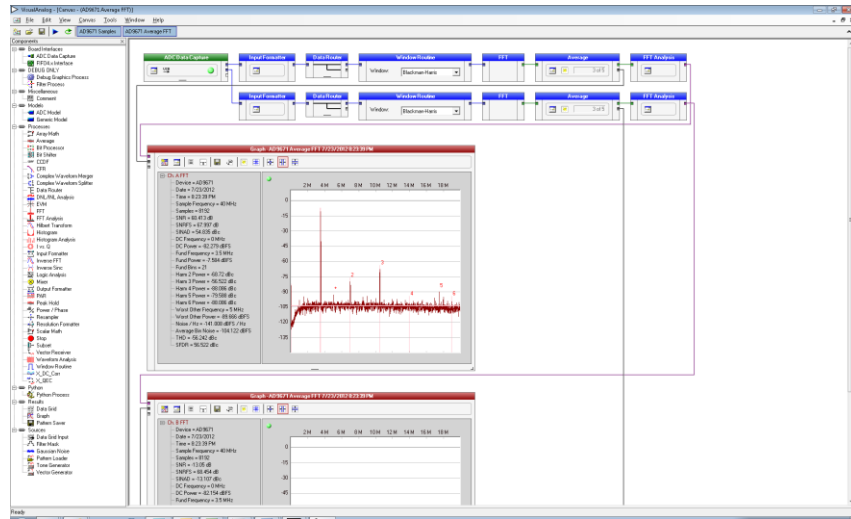


16. Selecting the blue right arrow on the VisualAnalog toolbar will run the canvas once and the green repeat button will set the canvas to run continually. The Sample Canvas will pop up two windows that show 8192 time domain samples for channels A and B.

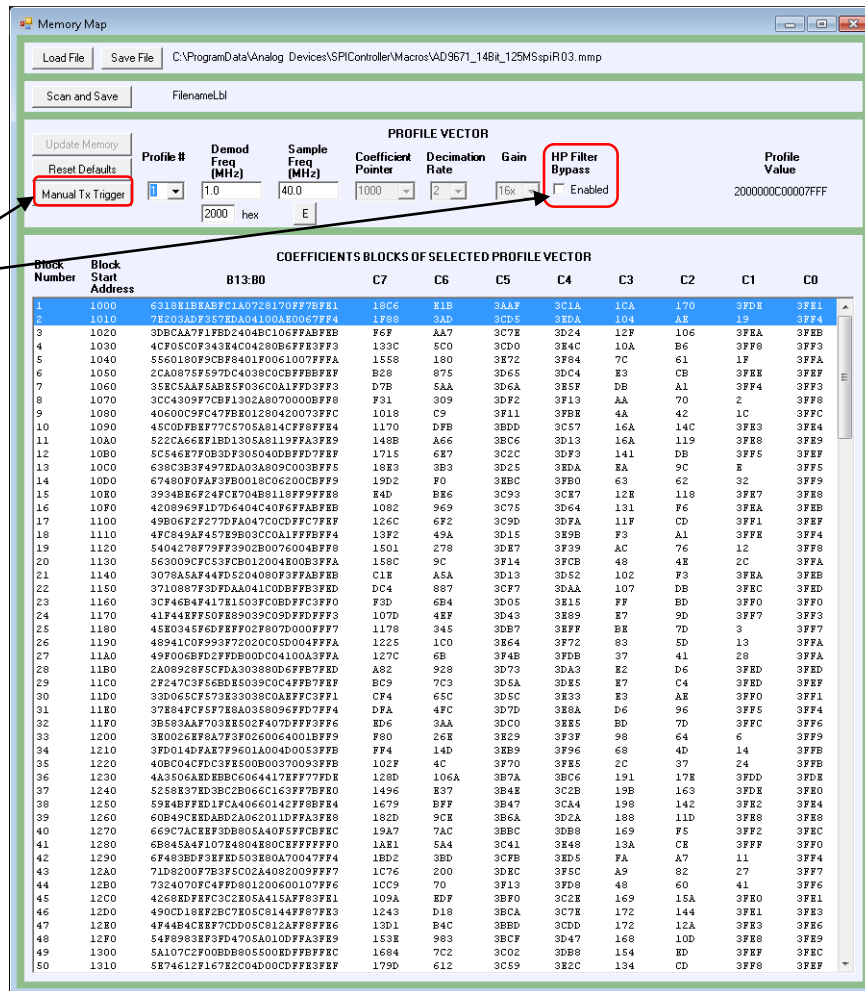


17. The AD9671_Average_FFT.vac canvas is setup for running and calculate FFT. The average count is set to 5 so the canvas either needs to be run 5 times or left in continuous run mode.

The result below shows the shaping of the noise floor as a result of the analog filters and the digital highpass filter.



18. The filter can be disabled through disabling it in the MemoryMap reader and running the Manual Tx Trigger.



19. The noise floor shape will now increase at low frequency with the removal the digital highpass filter.

